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Kebichi et al.
Application No. 09/872,212
SYNCHRONIZATION POINT ACROSS DIFFERENT MEMORY BIS
CONTROLLERS
Attorney Matter No. 1011-58140

FIG. 1

(PRIOR ART)

N MULTIPLE BIST CONTROLLERS WITH N MULTILPLE HOLD PINS

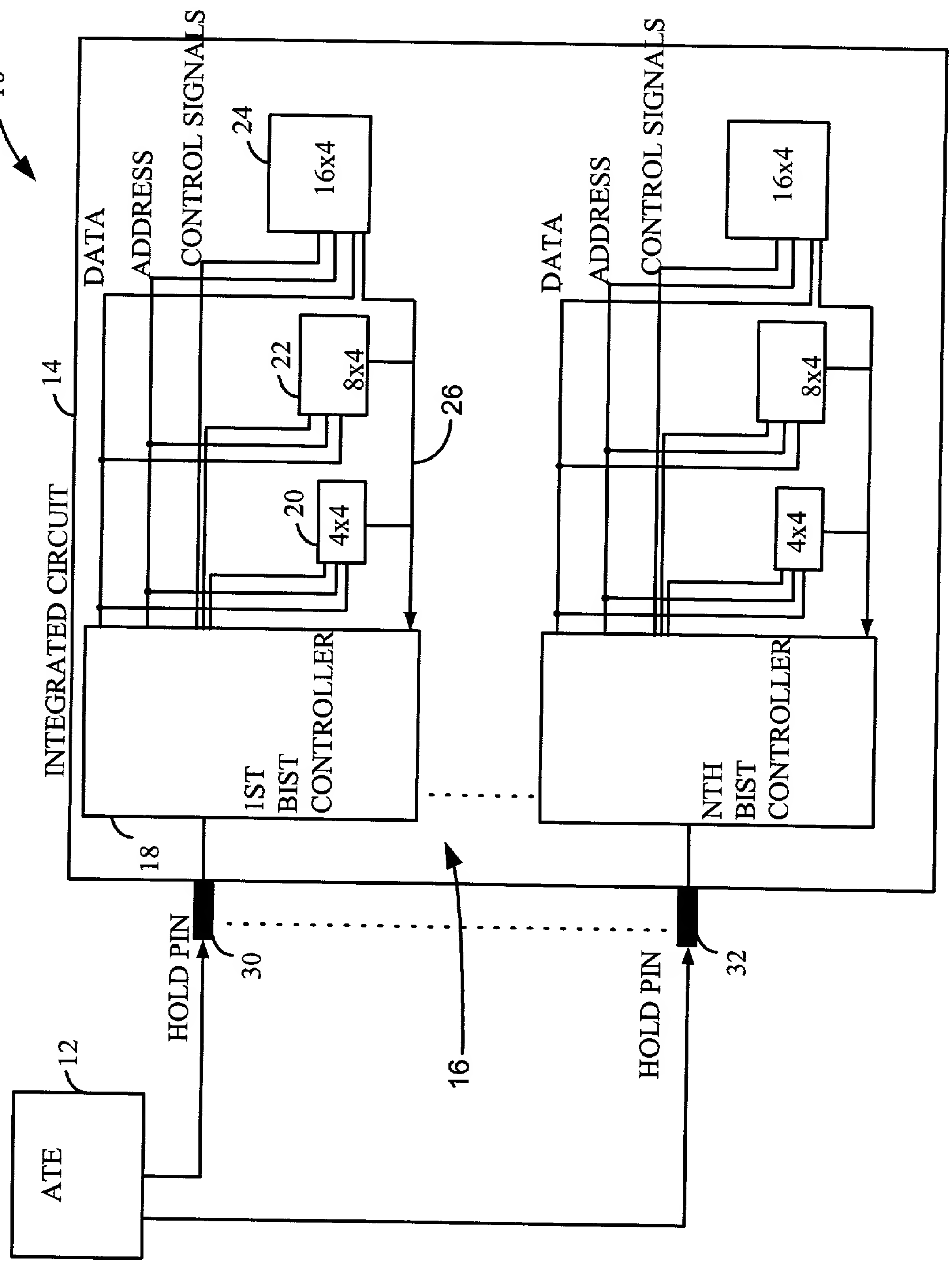
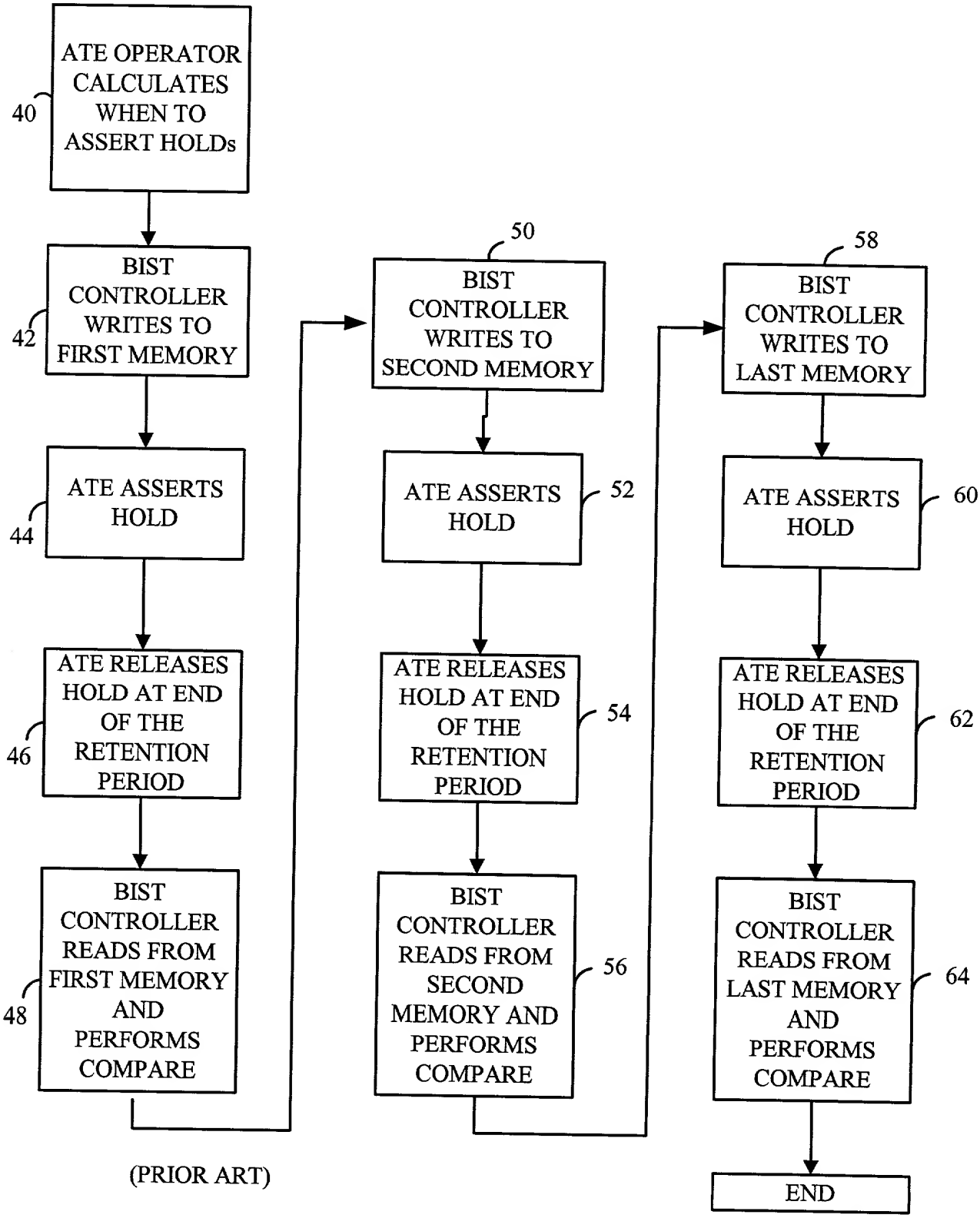


FIG. 2

TEST ON THREE MEMORIES COUPLED TO A SINGLE SEQUENTIAL BIST CONTROLLER USING THREE SEPARATE IDLE PERIODS



(PRIOR ART)

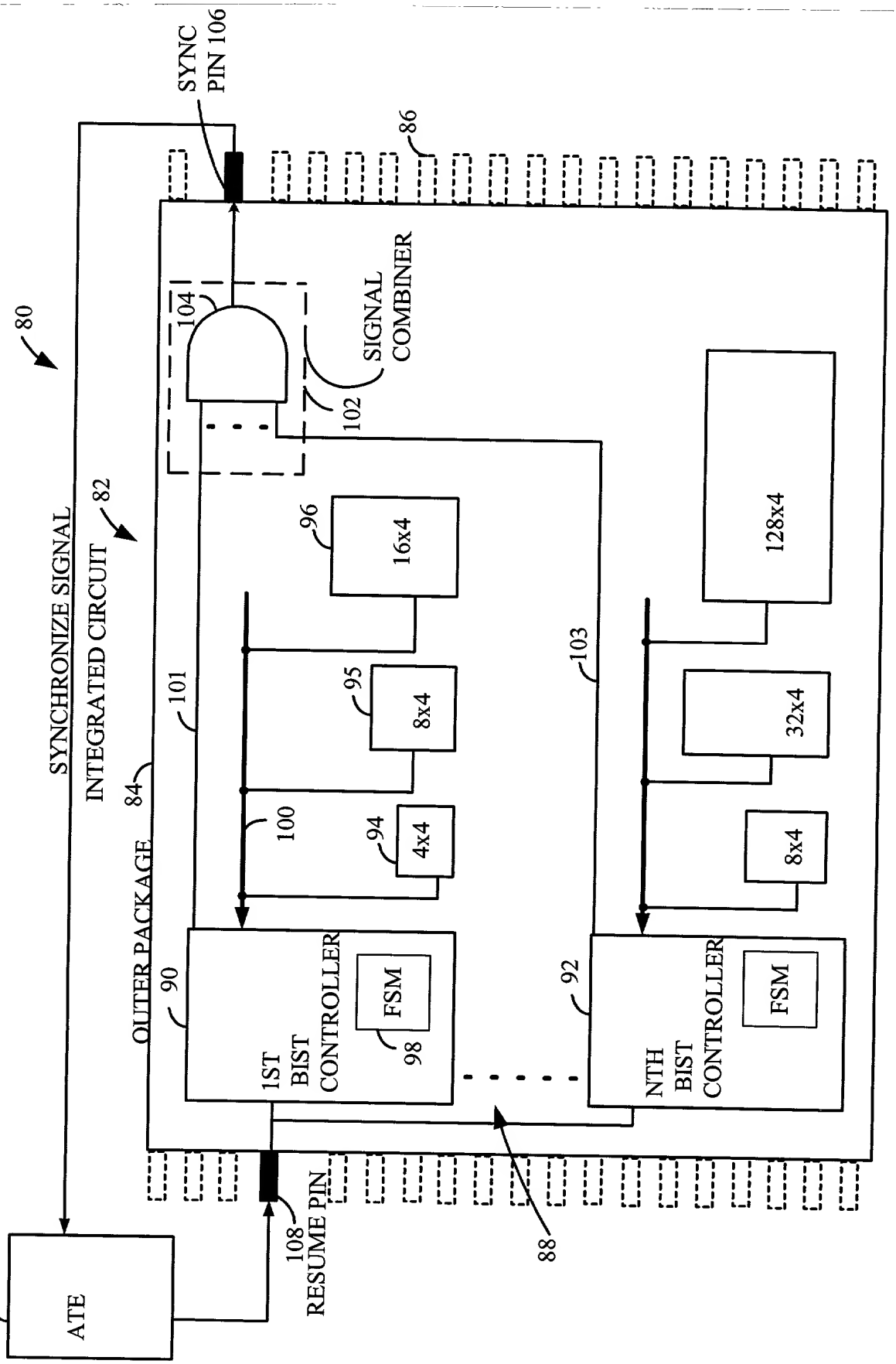


FIG. 3
N MULTIPLE BIST CONTROLLERS WITH SINGLE SYNCHRONIZE AND RESUME PINS

FIG. 4

TEST OF MEMORIES WITH MULTIPLE PARALLEL BIST CONTROLLERS USING SYNCHRONIZATION STATE

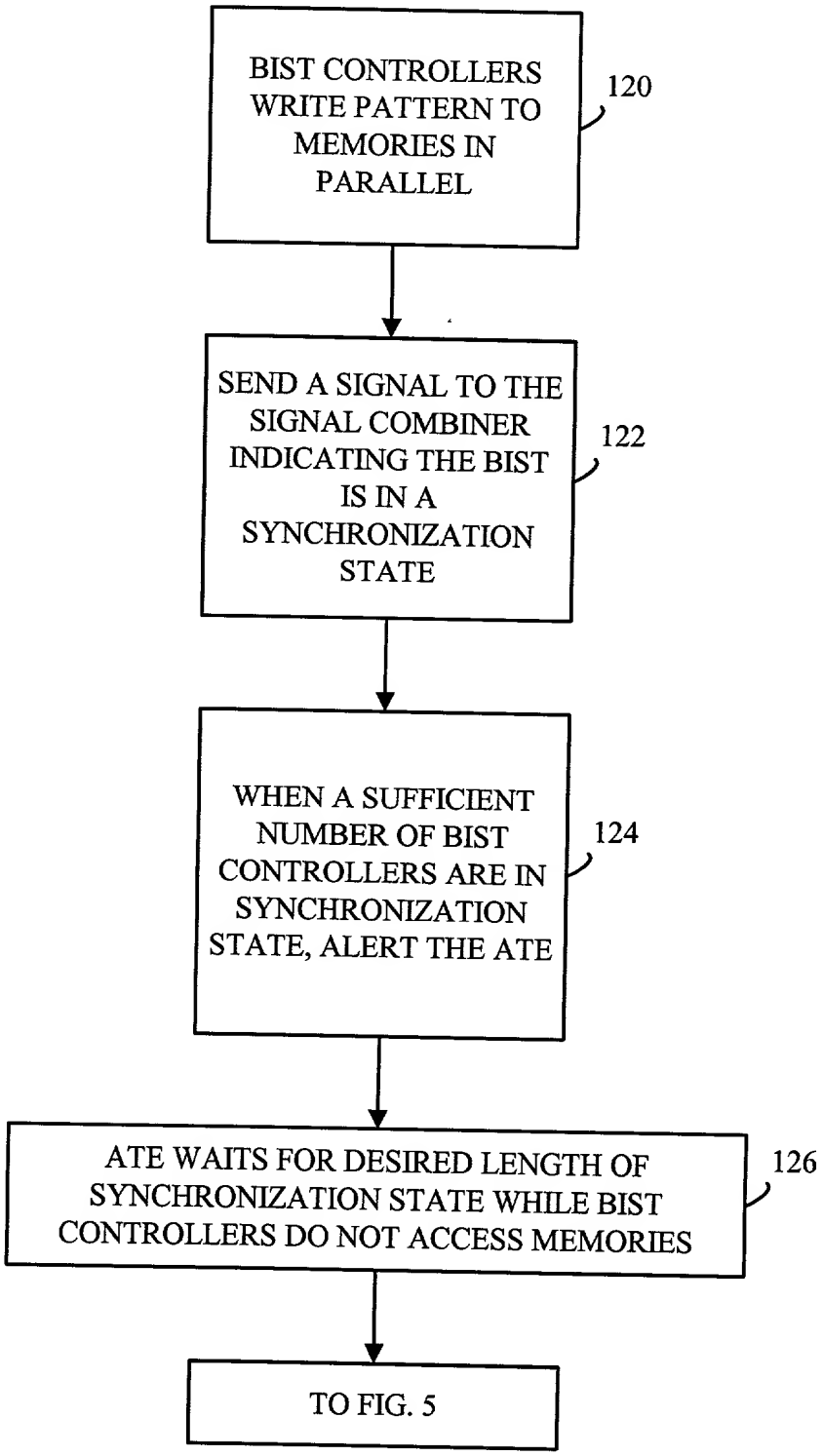


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FIG. 5

TEST OF MEMORIES WITH MULTIPLE PARALLEL BIST CONTROLLERS USING SYNCHRONIZATION STATE (CONTINUED)

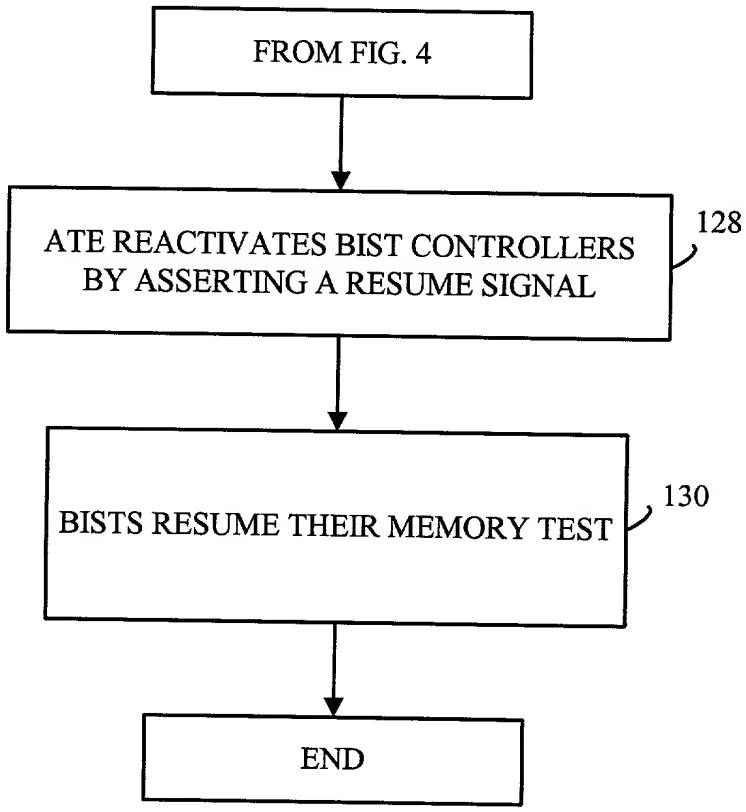

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FIG. 6

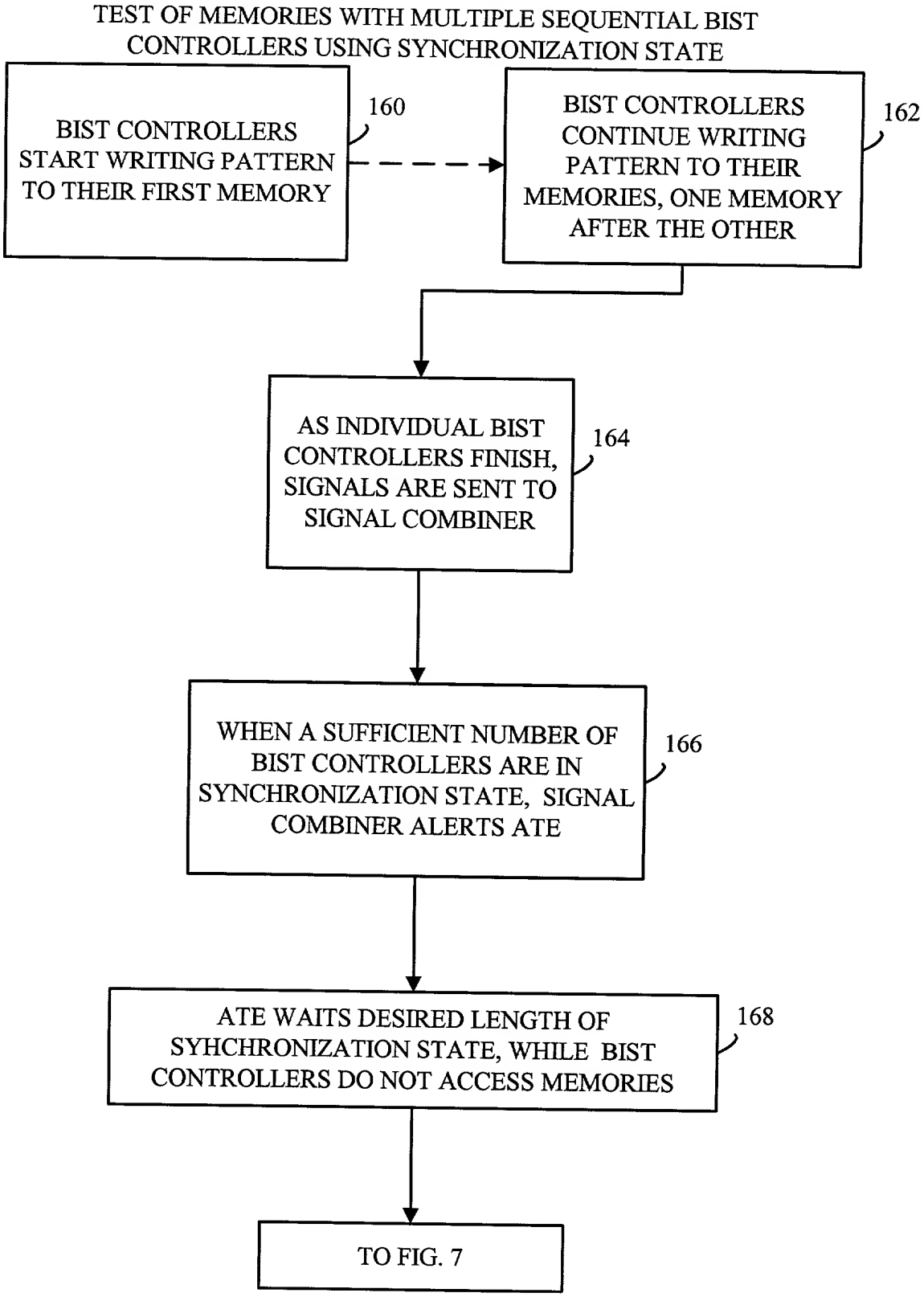

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FIG. 7

TEST OF MEMORIES WITH MULTIPLE SEQUENTIAL BIST CONTROLLERS USING SYNCHRONIZATION STATE (CONTINUED)

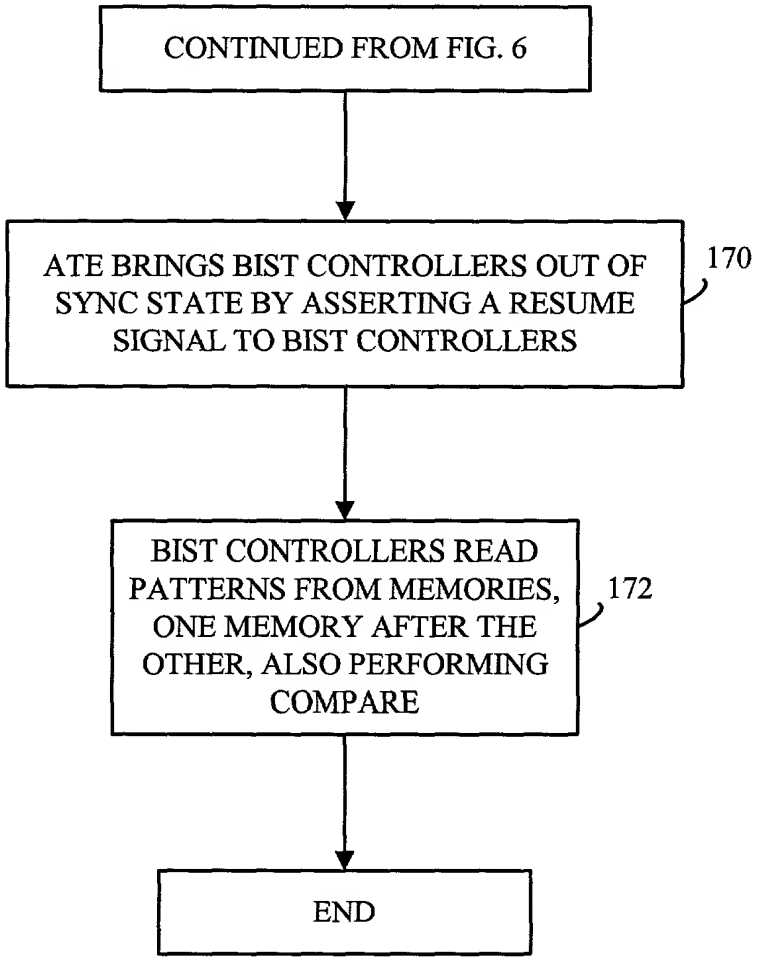

FIG. 8 — BIST CONTROLLER GENERATOR

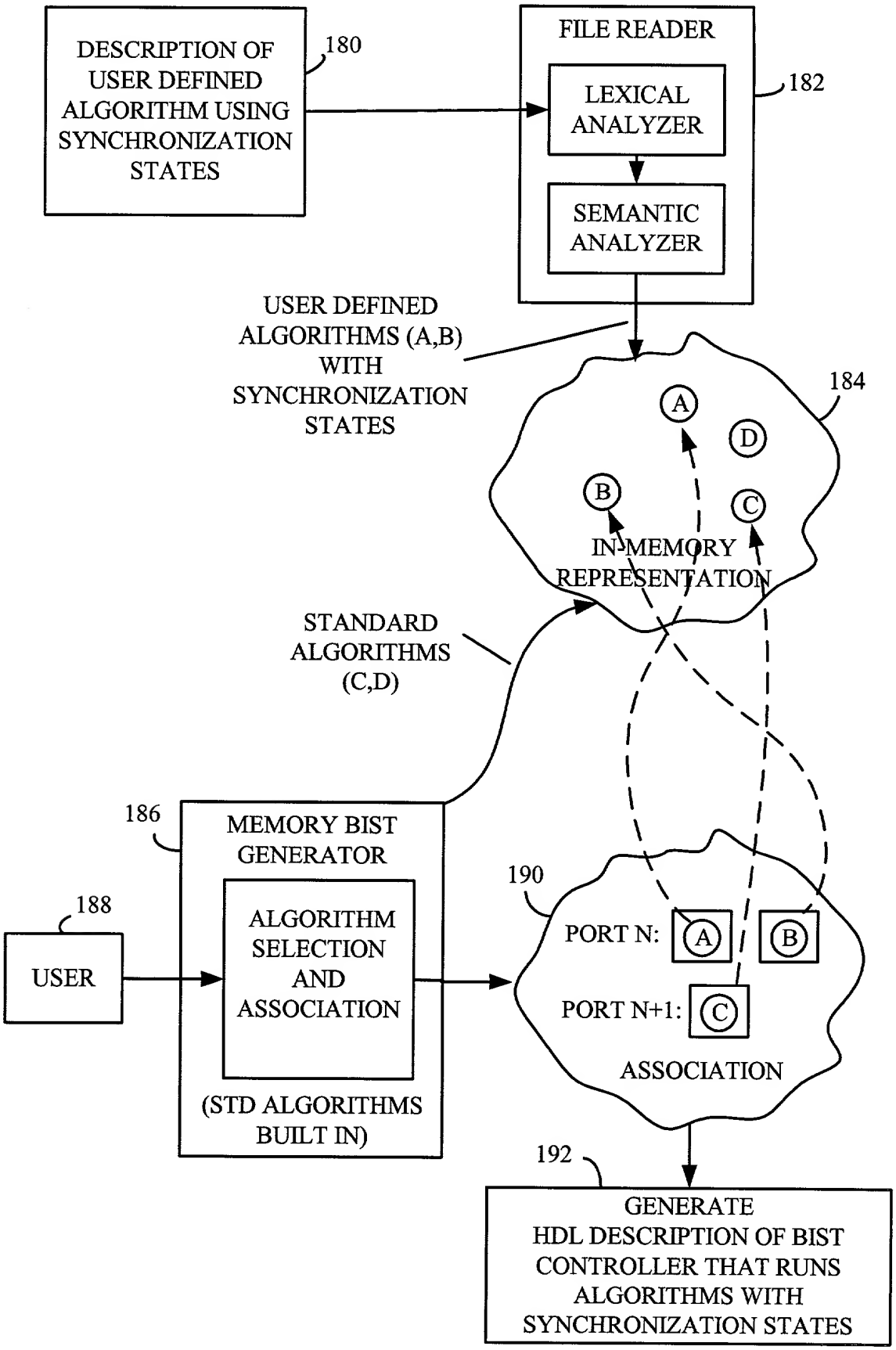

FIG. 9

GENERATING A BIST CONTROLLER THAT RUNS USER DEFINABLE ALGORITHIMS WITH SYNC KEYWORD